

Synergistic Modelling and Optimisation for Nanometre IC Design/Manufacturing Integration

GUEST SPEAKER

Prof. David Z. Pan

Department of Electrical and Computer Engineering
The University of Texas at Austin, TX 78712

When: **14th July 2009, 2.00 p.m. to 3.30 p.m.**

Where: **Institute of Microelectronics, Singapore (Level 2, Auditorium)**
11 Science Park Road Singapore Science Park II Singapore 117685

Abstract

Nanometre IC design and manufacturing are facing unprecedented grand challenges for 45nm and beyond, for performance, power, predictability, reliability, and so on. On one hand, many entangled physical effects continue to pose tremendous challenges to reach design closure with stringent turn-around-time; on the other hand, design closure no longer guarantees manufacturing closure. The conventional contracts between design and fab through design rules are breaking, due to deep sub-wavelength lithography and growing process variations. Thus design/manufacturing integration and co-optimisation will become more and more important. To enable true design/process integration, it is crucial to be able to model proper manufacturing/variability/yield metrics, and feed them upstream at various physical design implementation stages. This lecture will present synergistic modelling and optimisation issues on both physical and electrical design for manufacturing (DFM). We will seek to address DFM from its root causes, in a holistic manner through better manufacturing for design (e.g., variation aware lithography modelling and optical proximity correction), manufacturing-design interface (e.g., predictive silicon modelling and variation circuit analysis), and true "design" for manufacturing (i.e., manufacturability aware and variation tolerant designs).

Speaker Biography



Prof. David Z. Pan is an Associate Professor at the Department of Electrical and Computer Engineering, University of Texas at Austin, where he directs the UT Design Automation (UTDA) Lab. He received his Ph.D. in computer science (with honour) from UCLA in 2000. He was a Research Staff Member at IBM T. J. Watson Research Centre from 2000 to 2003. His research is mainly focused on nanometre physical design and design for manufacturability. He is also interested in physical and system-level co-design and design/CAD for emerging technologies. He holds 6 US patents and has published over 100 technical papers. He has served as an Associate Editor for IEEE Transactions on CAD (2006-), IEEE Transactions on VLSI Systems (2007-), IEEE Transactions on CAS-I (2008-), IEEE Transactions on CAS-II (2006-2007), and IEEE CAS Society Newsletter (2007-). He is on the DFM committee of the International Technology Roadmap for Semiconductor (ITRS). He has served in the program committees of major VLSI/CAD conferences including DAC, ICCAD, ASPDAC, DATE, ISPD, ISQED, and ISCAS. He is the 2009 IEEE CEDA/CASS CANDE Committee Chair, Program/General Chair for ISPD 2007/2008, CAD Track Co-Chair for ISCAS 2006 and 2007. He has received a number of awards for his research contributions and professional services, including the ACM/SIGDA Outstanding New Faculty Award (2005), NSF Career Award (2007), SRC Inventor Recognition Awards twice (2000 and 2008), IBM Faculty Award thrice (2004 to 2006), UCLA School of Engineering Distinguished Young Alumnus Award (2009), IBM Research Bravo Award (2003), 7 Best Paper Awards or Nominations from various international conferences (ASPDAC, DAC, ICCAD, ICICDT, and SRC Techcon), ISPD 2007 Global Routing Contest Awards, eASIC Placement Contest Grand Prize (2009), and ACM Recognition of Service Award (2007 and 2008). He is a Senior Member of IEEE and a Technical Advisory Board member of Pyxis Technology, Inc.

Registration

Pre-registration required. Please send the following details through email to:
Ms. Daphne Khong E-mail: khongkw@scei.a-star.edu.sg

Closing Date: Monday, 13th July 2009

Name			
Designation			
Company Name			
Address			
Tel		Fax	
Email			

Location Map

